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L13	switching adj1 device	91282	L13
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L9	L8 and l3	1	L9
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L4	test adj1 mode	19888	L4

L3	L2 and l1	57	L3
L2	secondary adj1 sense adj1 amplifier	122	L2
L1	primary adj1 sense adj1 amplifier	86	L1

END OF SEARCH HISTORY

L5: Entry 1 of 4 File: USPT Apr 5, 2005

DOCUMENT-IDENTIFIER: US 6876557 B2
** See image for Certificate of Correction **
TITLE: Unified SRAM cache system for an embedded DRAM system having a micro-cell architecture

Brief Summary Text (6):
The wide internal bus is used for facilitating a high data transfer rate among eDRAM, SRAM, and the processor(s). More specifically, data residing in eDRAM memory cells coupled to a wordline traversing an eDRAM block is transferred to primary sense amplifiers. The data is then transferred to corresponding secondary sense amplifiers. The data is then transferred to the first SRAM macro, i.e., the SRAM cache, and stored in the memory cells thereof at the same wordline location.

Brief Summary Text (9):
A fourth SRAM macro can be used for BIST operation. For example, the addresses of defective column or row elements must be temporarily recorded during a test mode. At the end of the test mode, when the redundancy algorithm is satisfied, the recorded addresses are used to program the fuses.

Brief Summary Text (10):
Finally, another SRAM macro may be required to store a portion of a test program for executing the test mode. Generally, there are two sets of test programs. The first set of programs are those fixed programs used to test the memory. This set is typically stored in a ROM. The second set of programs are those programmable programs used to test customized memory, or to provide test flexibility. This set is stored in SROM (scannable ROM). Similar to a fuse register array, the SROM is not an area efficiency design. The SROM can be replaced with an SRAM macro.

Detailed Description Text (9):
The SRAM cache 113, the fuse information caches 108A, 108B, and test program code cache (not shown) are never accessed simultaneously. That is, only when the bank address of the incoming address 103 and the bank address of the TAG block cache 104 do not match are the fuse information caches 108A, 108B accessed. Also, only during the test mode are test programs stored in the test program code cache needed. Therefore, the SRAM cache 113, the fuse information caches 108A, 108B, and test program cache are mutually exclusive. Accordingly, they can share the same set of bitlines during the same clock cycle.

Detailed Description Text (12):
The dual-port fuse information cache 204 can be used for redundancy allocation during the test mode and for storing fuse information during a redundancy test. That is, the fuse information cache 204 is configured for allocating redundant elements during the test mode and for storing fuse information during the redundancy test. During the test mode, the fuse information is streamed out from the fuse information cache 204 to hard program the fuse elements in case the fuse elements are determined to be faulty or defective.

Detailed Description Text (13):
When the test mode is over, the fuse information cache 204 is used to store the fuse information after each power-on for performing eDRAM read and write

L5: Entry 2 of 4 File: USPT Apr 1, 2003

DOCUMENT-IDENTIFIER: US 6542973 B2
TITLE: Integrated redundancy architecture system for an embedded DRAM

Abstract Text (1):
An integrated redundancy eDRAM architecture system for an embedded DRAM macro system having a wide data bandwidth and wide internal bus width is disclosed which provides column and row redundancy for defective columns and rows of the eDRAM macro system. Internally generated column and row addresses of defective columns and rows of each micro-cell block are stored in a memory device, such as a fuse bank, during an eDRAM macro test mode in order for the information to be quickly retrieved during each cycle of eDRAM operation to provide an SRAM-like operation. A column steering circuit steers column redundant elements to replace defective column elements. Redundancy information is either supplied from a SRAM fuse data storage device or from a TAG memory device depending on whether a read or write operation, respectively, is being performed. The integrated redundancy eDRAM architecture system enables data to be sent and received to and from the eDRAM macro system without adding any extra delay to the data flow, thereby protecting data flow pattern integrity.

Brief Summary Text (5):
In order to effectively utilize the large DRAM cache size, a small SRAM unit about the same size of an eDRAM block is used. The SRAM unit serves as a cache interface between an eDRAM and processor(s). The wide internal bus is used for transferring data among eDRAM, SRAM and the processor(s). More specifically, data residing in eDRAM memory cells coupled to a wordline traversing an eDRAM block is transferred to primary sense amplifiers. The data is then transferred to corresponding secondary sense amplifiers. The data is then transferred to the SRAM and stored in the memory cells thereof at the same wordline location. A TAG memory records the block address of the data stored within the SRAM. The data is then transferred to the processor(s).

Brief Summary Text (15):
Accordingly, an integrated redundancy eDRAM architecture system for an embedded DRAM macro system having a wide data bandwidth and wide internal bus width is disclosed which provides column and row redundancy for defective columns and rows of the eDRAM macro system. Internally generated column and row addresses of defective columns and rows of each micro-cell block are stored in a memory device, such as a fuse bank, during an eDRAM macro test mode in order for the information to be quickly retrieved during each cycle of eDRAM operation to provide an SRAM-like operation. A column steering circuit steers column redundant elements to replace defective column elements. Redundancy information is either supplied from an SRAM fuse data storage device or from a TAG memory device depending on whether a read or write operation, respectively, is being performed. The integrated redundancy eDRAM architecture system enables data to be sent and received to and from the eDRAM macro system without adding any extra delay to the data flow, thereby protecting data flow pattern integrity.

Detailed Description Text (3):
With reference to FIG. 1, there is shown a block diagram of an exemplary prior art eDRAM macro system having a micro-cell architecture and designated generally by

reference numeral 100. The eDRAM macro system 100 includes a plurality of one mega-byte micro-cell blocks, e.g., micro-cell blocks #1M block, #2M block, #3M block, . . . , #32M block. Each mega-byte micro-cell block includes eight banks, e.g., bank BNK. Depending on the application, a typical eDRAM macro may include 64 to 512 banks. Each bank includes four micro-cells, e.g., micro-cell MCB. Each micro-cell includes 258 wordlines, where two wordlines are redundant wordlines RWL, and 152 bitline pairs, where eight bitline pairs are redundant bitline pairs RBL. Wordline decoder/driver circuitry WDD is used to activate the wordlines. A primary sense amplifier block PSA is provided for each micro-cell and a secondary sense amplifier block SSA is provided for each bank.

Detailed Description Text (14):
The column and row redundancy information is originally recorded in the fuse bank which may reside within or outside the eDRAM macro system 100. The information indicates the failed column and row address bits which were determined during a test mode of the eDRAM macro system 100. It is contemplated that the failed column and row address bits determined during the test mode can be stored in the TAG memory device 200 or in another memory device, such as an SRAM fuse data storage memory device 300 described below.

Detailed Description Text (20):
To accomplish this task, 36 switches or multiplexers 402.sub.1-36 and two decoders 404, 406 for receiving data from the SRAM fuse data storage device 300 are provided. Each switch 402 selects one of three groups, i.e., the one column group of incoming datalines DLs corresponding to each respective switch 402 or one of the two redundancy column groups of incoming datalines RDLs, according to the inputs received from the two decoders 404, 406. For example, the first and the second switches 402.sub.1, 402.sub.2 each select at most one of the 36 groups of four incoming datalines DLs to be replaced by the redundancy column group of datalines RDLs depending on the incoming six bits of column fuse information supplied by the SRAM fuse data storage device 300 via the two decoders 404, 406. Within each switch 402, either the first or the second redundancy column group of incoming datalines RDLs is selected. The fuse information is determined during the test mode of the eDRAM macro system 100 as indicated above.

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operations. The stored fuse information is accessible by the eDRAM system during a non-test mode, e.g., during the execution of read and write operations, for selecting available redundant elements as indicated by the stored fuse information to replace defective elements to direct data to and from the eDRAM array 115.

CLAIMS:

11. The system according to claim 10, wherein the fuse information cache is configured for allocating redundant elements during a test mode, for storing fuse information during a redundancy test, and for being accessible by the eDRAM system for selecting available redundant elements as indicated by the stored fuse information to replace defective elements.

23. The system according to claim 22, wherein the fuse information cache is configured for allocating redundant elements during a test mode, for storing fuse information during a redundancy test, and for being accessible by the eDRAM system for selecting available redundant elements as indicated by the stored fuse information to replace defective elements.

30. The system according to claim 27, wherein the fuse information cache is configured for allocating redundant elements during a test mode, for storing fuse information during a redundancy test, and for being accessible by the eDRAM system for selecting available redundant elements as indicated by the stored fuse information to replace defective elements.

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L5: Entry 3 of 4 File: USPT May 4, 1999

DOCUMENT-IDENTIFIER: US 5901105 A
** See image for Certificate of Correction **
TITLE: Dynamic random access memory having decoding circuitry for partial memory blocks

Drawing Description Text (17):
FIG. 15 is a schematic diagram of a portion of the memory device of FIG. 2 including bitlines and primary sense amplifiers therein;

Drawing Description Text (18):
FIG. 16 is a schematic diagram of a primary sense amplifier from the memory device of FIG. 2;

Drawing Description Text (58):
FIG. 56 identifies the names of input and output signals to test mode logic circuitry in the memory device of FIG. 2;

Drawing Description Text (59):
FIG. 57 is a schematic diagram of a portion of the test mode logic circuitry in the memory device of FIG. 2, including a supervoltage detector circuit;

Drawing Description Text (61):
FIG. 59 is a schematic diagram of another portion of the test mode logic circuitry in the memory device of FIG. 2;

Drawing Description Text (62):
FIG. 60 is a schematic diagram of another portion of the test mode logic circuitry in the memory device of FIG. 2;

Drawing Description Text (63):
FIG. 61 is a table listing test mode addresses for the memory device of FIG. 2;

Drawing Description Text (65):
FIG. 63 is a table listing read data and outputs for test modes of the memory device of FIG. 2;

Drawing Description Text (152):
FIG. 150 is a schematic diagram of a portion of row redundancy circuitry associated with the test mode of the memory device of FIG. 2;

Drawing Description Text (207):
FIG. 205 is a table identifying ignored column addresses for test mode compression in the memory device of FIG. 2;

Drawing Description Text (213):
FIG. 211 is a table relating to test mode compression addresses in the memory device of FIG. 2;

Detailed Description Text (22):
Turning now to FIG. 13, which is a schematic representation of a typical quadrant

12 of DRAM 10, it can again be seen that each 16 Mbit quadrant 12 consists of two 8 Mbit sections or PABs 14L and 14R mirrored about a column block 30. Each column block 30 drives four pairs of data read (DR) lines 50 and four data write (DW) lines 52. As shown in FIG. 13, column block 30 includes a plurality of DC sense amplifiers (DCSAs) 56 which are coupled to so-called secondary I/O lines 58 extending laterally along 8 Mbit PABs 14L and 14R. Secondary I/O lines 58, in turn, are multiplexed by multiplexers 60 to sense amplifier output lines 62, also referred to herein as local I/O lines. Local I/O lines 62 are coupled to the outputs of primary sense amplifiers 64 and 65, whose inputs are coupled to bit lines 66. This arrangement can perhaps be better appreciated with reference to FIG. 14, which depicts a portion of an 8 Mbit PAB 14 including a section 20 of columns and a section 18 of rows.

Detailed Description Text (29):
The even digit line pairs D0/D0*, D2/D2*, D4/D4*, and D6/D6* are coupled to the left or even primary sense amplifiers designated 64 in FIG. 14, while the odd bit line pairs D1/D1*, D3/D3*, D5/D5*, and D7/D7* are coupled to right or odd primary sense amplifiers. 65. The even or odd sense amplifiers 64/65 are alternatively selected by the least significant bit of the column address (CA0), where CA0=0 selects the even primary sense amplifiers 64 and CA0=1 selects the odd primary sense amplifiers 65.

Detailed Description Text (41):
In a test mode in which 1s are written to each cell in the array, the arrangement of comparators 73, 74, and 75 results in a situation in which the outputs from four DC sense amplifiers 56 are reflected by the output from a single comparator 75. If all four DC sense amps 56 associated with a comparator 75 are reading 1s, the output from that comparator 75 will be a 1; if any of the four DC sense amps 56 is reading a zero, the output from that comparator 75 will also be zero. In this way, a 4:1 test data compression is achieved.

Detailed Description Text (46):
The circuitry that is disposed in the gaps 104 which exist as a result of the hierarchical row decoding arrangement in accordance with the present invention is shown in greater detail in FIGS. 160 through 163. Notably, gaps 104 serve as a convenient location of multiplexers 60 (see FIG. 14) which operate to selectively couple the outputs of primary sense amplifiers 64 or 65 to local I/O lines 58. A typical one of multiplexers 60 is shown in schematic form in FIG. 162.

Detailed Description Text (72):
The SVFID* input signal also required to enable FUSEID fusebank 610 is generated by the test mode logic circuitry of FIG. 57, 59, and 60 in response to a supervoltage being detected on address input pin 7 accompanying a WCBR cycle.

Detailed Description Text (88):
Returning to FIG. 52, it is also apparent therefrom that assertion of RASD also leads to assertion of an active low signal RAEN*, which signal activates row address predecoders 110, 112, 114, 116, 118, 120, 122, and 124, as shown in FIG. 19. Assertion of RAEN* also leads to deassertion of the signals ISO and EQ, as is apparent from the EQ control and ISO control circuitry of FIG. 54. Deassertion of ISO and EQ isolates non-accessed arrays by turning off isolation devices 84L and 84R in primary sense amplifiers 64, and discontinues equalization of digit lines 71 by turning off equalization devices 90L and 90R, as is apparent in the schematic of FIG. 16.

Detailed Description Text (96):
TEST MODE LOGIC

Detailed Description Text (97):
DRAM 10 is in accordance with the presently disclosed embodiment of the invention

is capable of being operated in a test mode wherein it can be determined, for example, whether defects in the integrated circuit make it necessary to switch-in certain redundant circuits (rows or columns). Some of the circuitry associated with this test mode of DRAM 10 is depicted in FIGS. 56 through 63.

Detailed Description Text (98):
One notable aspect of the test mode circuitry relates to the supervoltage detect circuit 960 shown in FIG. 57. Supervoltage detect circuits similar to that shown in FIG. 57 are used in various portions of the circuitry of device 10, to detect voltage levels applied to input pins of the device which are higher than the standard logic-level (e.g., 0 to 3.3 or 5 volts) signals normally applied to those inputs. Supervoltages are applied in this manner 10 to trigger device 10 temporarily into different modes of operation, for example, fuse programming modes, test modes, etc., as will be hereinafter described in further detail.

Detailed Description Text (124):
The even bit line pairs D0/D0* and D2/D2* are coupled to left or even primary sense amplifiers 64. The odd bit line pairs D1/D1* and D3/D3* are coupled to right or odd primary sense amplifiers 65. The even or odd sense amplifiers are alternatively selected by the least significant bit of the column address CA0, where CA0=0 selects the even primary sense amplifiers 64 and CA0=1 selects the odd primary sense amplifiers 65. The four even bit line pairs D0/D0* and D2/D2* are further coupled to two sets of I/O lines that proceed to secondary DC sense amplifiers 80. Likewise, the four odd bit line pairs D1/D1* and D3/D3* are coupled to a different two sets of I/O lines which are connected to secondary DC sense amplifiers 56, as described above with reference to FIGS. 13 and 17. The secondary DC sense amplifiers 56 are coupled via the same data line to a data I/O buffer.

Detailed Description Text (173):
(Each of the inputs pa<0:3> through pf<0:3> to redundant laser fuse match circuits 270 are coupled to either signal line p 766 or to signal line pr 768 terminals shown in FIG. 79. During normal operation of device 10, terminals p 766 and pr 768 are always both tied to V.sub.cc or both tied to ground, depending upon whether enable fuse 748 is not blown or blown, respectively, to enable row laser fusebank 250. Thus, the signals pa<0:3> through pf<0:3> are likewise all either at V.sub.cc or all at ground, depending upon whether enable fuse 748 is blown or not blown. The reason the signals pa<0:3> through pf<0:3> are differentiated is in support of a redundancy test mode, in which it is desirable to temporarily map each fusebank 250 to an address without blowing enable fuse 748 for the purposes of testing the redundant rows, i.e., simulating a situation in which the fusebank 250L is enabled and a row address is applied to cause a critical address match without blowing fuses in the fusebank 250L.

Detailed Description Text (179):
In FIG. 76, it can be seen that each row electrical fusebank 250E includes an electrical fusebank enable circuit 261 having an enable fuse 748. Enable fuse 748, like enable fuse 748 in FIG. 79, is blown to activate or enable the fusebank 250E with which it is associated. When enable fuse 748 is blown, this causes assertion of the electrical fuse enable signal designated EFEN in FIGS. 76, 77, and 78 to activate electrical fusebank 250. In particular, the EFEN signal which is asserted in response to the blowing of enable fuse 748 in row electrical fusebanks 250, is applied to one input of NAND gates 810, 812, 184, and 816 included in each row redundant electrical fuse match circuit 270 in each row electrical fusebank 250. When the EFEN input to each NAND gate 810, 812, 814, and 816 is deasserted, the outputs from those NAND gates will always be high. When enable fuse 748 in a row electrical fusebank 250 is blown, however, the EFEN input to each NAND gate 810, 812, 814, and 816 will be asserted, so that those NAND gates each act as inverters with respect to the other input thereof. The assertion of the EFEN output from electrical row fuse enable circuit 261 also is determinative of the assertion or deassertion of the p and pr outputs 766 and 768 from redundant row pulldown

circuits 268 and 269 in FIG. 76. Like the p and pr outputs 766 and 768 in row laser fusebank circuits in FIG. 79, the p and pr outputs 766 and 768 from redundant row pulldown circuits 268 and 269 in FIG. 76 determine whether the pa<0:3> through pf<0:3> inputs to redundant row fuse match circuits 255 in row electrical fusebanks 250 are asserted or deasserted. As was the case for the pa<0:3> through pf<0:3> signals in FIG. 279, those in FIGS. 77 and 78 are either all asserted or all deasserted, depending upon whether enable fuse 748 is or is not blown, except during a redundant row test mode of operation, in which individual electrical row fusebanks 250 are mapped to particular addresses for the purposes of testing. If enable fuse 748 is not blown, the signals pa<0:3> through pf<0:3> will always be asserted, preventing the m*<x> outputs from electrical row fuse match circuit 255 from ever being asserted (low). When enable fuse 748 is blown, on the other hand, (and device 10 is not operating in the redundant row test mode) the pa<0:3> through pf<0:3> signals are all deasserted, so that depending upon which electrical antifuses 257 are blown, each row electrical fusebank 250 will be responsive to a unique local row address applied to its RAxy<z> inputs to its electrical row fuse match circuits 253 to assert (low) its m*<x> outputs. If a row address for which a given row electrical fusebank 250 is programed is applied, each of its m*<x> outputs will be asserted (low), so that the RBmPHn output from its row redundant match circuit 257 will be asserted (high).

Detailed Description Text (195):
The invention is readily adaptable to provide parallel redundancy between two or more sections during test mode address compression. In this way, one set of match-fuse banks would govern the replacement of a primary row with a specific redundant row in a first section and the same replacement in a second section. This allows for speedier testing and repair of the memory chip.

Detailed Description Text (203):
As shown in FIG. 76, the EFEN signal is ORed with a signal REDTESTR in OR gate 266 to generate an active low enable fusebank signal ENFB* (the ORing of EFEN with REDTESTR is done for purposes related to test modes in device 10, which is not relevant to the present description). The enable fusebank signal ENFB* is then ORed, in OR gate 267 in a redundant row pulldown circuit 268, to generate a pulldown signal p, and in a redundant pulldown circuit 269 to generate a pulldown signal pr.

Detailed Description Text (244):
An alternative embodiment of the invention is shown in FIG. 227. Recall from FIG. 2 that integrated circuit memory device 10 in accordance with the presently disclosed embodiment of the invention has four substantially identical quadrants 12, designated in FIG. 227 as 22-1, 12-2, 12-3, and 12-4. VCC 350, and GND 354 connections are provided to the functional elements through isolation devices 358-1, 358-2, 358-3, and 358-4. Control circuit 360 provides control and data signals to and from the functional elements via signal bus 380. After manufacture, device 10 is placed in a test mode. Methods of placing a device in a test mode are well known in the art and are not specifically described herein. A test mode is provided to electrically isolate one, some or all of the functional elements 12-1, 12-2, 12-3, and 12-4 from global supply signals VCC 350 and GND 354 via control signals from control circuit 360 over signal bus 380. The capability of individually isolating each of the functional elements 12-1, 12-2, 12-3, and 12-4 allows ease of test of the control and interface circuits 1360, as well as testing of each one of the functional elements 12-1, 12-2, 12-3, and 12-4 without interference from the others.

Detailed Description Text (250):
FIG. 231 shows an initialization circuit which when used as part of the present invention allows for automatically isolating defective circuit elements that draw excessive current when an integrated circuit is powered up. By automatically isolating circuit elements that draw excessive current, the device can be repaired

before it is damaged. A power detection circuit 420 is used to generate a power-on signal 422 when global supply signal 424 reaches a desired potential. Comparator 426 is used to compare the potential of global supply 424 with local supply 428. Local supply 428 will be of approximately the same potential as global supply 424 when the isolation device 430 couples global node 424 to local node 428 as long as the circuit element 432 is not drawing excessive current. If circuit element 432 does draw excessive current, the resistivity of the isolation device 430 will cause a potential drop in the local supply 428, and the comparator 426 will output a high level on signal 434. Power-on signal 422 is gated with signal 434 in logic gate 436 so that the comparison is only enabled after power has been on long enough for the local supply potential to reach a valid level. If signals 438 and 440 are both inactive high, then signal 442 from logic gate 790 will pass through gates 444 and 446 and cause isolation signal 448 to be low, which will cause the isolation device 430 to decouple the global supply from the local supply. Isolation signal 440 (ISO*) can be used to force signal 448 low regardless of the output of the comparator as long as signal 438 is high. Signal 440 may be generated from a test mode, or from a programmable source to isolate circuit element 432 for repair or test purposes. Test signal 81 may be used to force the isolation device 430 to couple the global supply to the local supply regardless of the active high disable signal 450. Signal 438 is useful in testing the device to determine the cause of excessive current draw. In an alternate embodiment, multiple isolation elements may be used for isolation device 430. On power up of the chip, a more resistive isolation device is enabled to pass a supply voltage 424 to the circuit 432. If the voltage drop across the resistive device is within a predetermined allowable range, then a second lower resistance isolation device is additionally enabled to pass the supply voltage 424 to circuit 432. This method provides a more sensitive measurement of the current draw of circuit 432. If the voltage drop across the resistive element is above an acceptable level, then the low resistance device is not enabled, and the resistive device can optionally be disabled. If the resistive device does not pass enough current to a defective circuit 432, it is not necessary to disable it, or even to design it such that it can be disabled. In this case a simple resistor is adequate.

CLAIMS:

4. A memory device in accordance with claim 3, further comprising:

a plurality of primary sense amplifiers, each primary sense amplifier disposed adjacent to at least one sub-array and responsive to application of a column select signal to said sub-array to sense a voltage differential on said digit lines in said array.

5. A memory device in accordance with claim 4, further comprising:

a plurality of secondary sense amplifiers, each disposed in one of said second type of intermediate areas and selectively coupled to said primary sense amplifiers via said secondary input/output lines.

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L5: Entry 4 of 4 File: DWPI Apr 15, 2004

DERWENT-ACC-NO: 2004-355154
DERWENT-WEEK: 200433

TITLE: Semiconductor dynamic RAM circuit reads out data by connecting switching devices in parallel based on test mode signal and bit line address, so that one of primary amplifiers is connected to assigned secondary amplifier

Basic Abstract Text (1):
NOVELTY - A test control unit (14) reads out data from the memory circuit by connecting the switching devices (8) in parallel based on a test mode signal (TM) and a read-out bit line address (BA), so that one of the primary sense amplifiers (5) is connected to the assigned secondary sense amplifier (6).

Basic Abstract Text (6):
primary sense amplifiers 5

Basic Abstract Text (7):
secondary sense amplifier 6

Basic Abstract Text (11):
test mode signal TM

Standard Title Terms (1):
SEMICONDUCTOR DYNAMIC RAM CIRCUIT READ DATA CONNECT SWITCH DEVICE PARALLEL BASED TEST MODE SIGNAL BIT LINE ADDRESS SO ONE PRIMARY AMPLIFY CONNECT ASSIGN SECONDARY AMPLIFY

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L12: Entry 1 of 2 File: USPT Oct 22, 2002

DOCUMENT-IDENTIFIER: US 6470465 B1
TITLE: Parallel test circuit of semiconductor memory device

Brief Summary Text (6):
Referring to FIG. 1, a conventional parallel test circuit is illustrated. As shown in FIG. 1, the parallel test circuit includes a data input pad DIN, to which data to be written is inputted, and a pair of cell arrays, that is, a first cell array 2A and a second cell array 2B, each consisting of a plurality of memory cells each adapted to store the data inputted to the data input pad DIN. Also, there is an output driver 8 which is switched, in accordance with respective data A and B stored in the first and second cell arrays 2A and 2B, between a normal mode, in which it outputs the stored data A and B, and a test mode in which it outputs a signal having a high or low level selected on the basis of the levels of the stored data A and B. The parallel test circuit also includes a first switch SW1 for selectively coupling the input data from the data input pad DIN to a normal path or a test path, a second switch SW2 for selectively coupling the data inputted via the normal path to the first cell array 2A or second cell array 2B in the normal mode, and a third switch SW3 for selectively outputting the first data A stored in the first cell array 2A or the second data B stored in the second cell array 2B via the normal path in the normal mode. The parallel test circuit further includes an inverter INV1 for inverting the data selectively outputted in accordance with a switching operation of the third switch SW3, an output driver control unit 4 for outputting a first output driver driving signal DR1 and a second output driver driving signal DR2 adapted to control an output driver 8 in the test mode, based on the data A and B from the first and second cell array 2A and 2B, respectively, and a fourth switch SW4 for selectively coupling the data selectively outputted in accordance with the switching operation of the third switch SW3 or the first output driver driving signal DR1 from the output driver control unit 4 to the output driver 8. The parallel test circuit also includes a fifth switch SW5 for selectively coupling the output from the first inverter INV1 or the second output driver driving signal DR2 from the output driver control unit 4 to the output driver 8, and a data output pad DOUT for externally outputting the output from the output driver 8 when the data is to be read.

Brief Summary Text (21):
In accordance with an embodiment of the present invention, each of the first and second comparing means is a current mirror type sense amplifier.

Detailed Description Text (36):
The sub output driver control unit 6E includes a fourth inverter INE4 for inverting the output enable signal OE, a NOR gate NORE for NORing the output from the fourth inverter INE4 with the output signal CONE from the main output driver control unit 4E. The sub output driver control unit 6E also includes a first current mirror type sense amplifier SA1 activated by the output from the NOR gate NORE and adapted to compare the output data from the sub output driver 10E with a first reference voltage VREF1, thereby outputting a first sub driving signal SDRE1. The sub output driver control unit 6E further includes a second current mirror type sense amplifier SA2 activated by the output from the NOR gate NORE and adapted to compare the output data from the sub output driver 10E with a second reference voltage VREF2, thereby outputting a second sub driving signal SDRE2, and a fifth inverter

INE5 for inverting the output from the second sense amplifier SA2, thereby outputting the second sub driving signal SDRE2.

CLAIMS:

7. The parallel test circuit in accordance with claim 6, wherein each of the first and second comparing means is a current mirror type sense amplifier.

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L16: Entry 1 of 3 File: USPT Nov 1, 2005

DOCUMENT-IDENTIFIER: US 6961273 B2
TITLE: RAM memory circuit having a plurality of banks and an auxiliary device for testing

Detailed Description Text (10):
The test mode setting signal TM may be kept inactive in the normal operating mode of the memory circuit. Under this condition, the selection parallel switching device 34 is inactive, and the test control signal transmitter 35 keeps the test control signals S1 and S2 inactive, so that the switch 32 remains closed, that the bus parallel switching device 33 remains inactive and that the evaluation devices 30[A:D] are all deactivated. A bank address BAD, a row address RAD and a column address CAD are applied via external address terminals to activate the selection device of the bank determined by the bank address BAD, so that the memory cell group (n=16 memory cells) of only this bank is selected, which group is determined by the addresses RAD and CAD. At the same time, the bank multiplexer 25 may be set by the bank address BAD such that the bank bus (e.g., of precisely the respective bank) is connected to the data port 24 (via the n-pole switch 32 that is closed in the normal mode). Consequently, a data transfer path for the parallel inputting of n write data or for the parallel outputting of n read data at the selected bank is produced between the n external data terminals D[0:15] and the n selected memory cells. The temporal sequence of the different switching operations in the respectively activated selection device for writing and reading is controlled by corresponding timing control signals which are generated in the control unit 26 under the influence of the write control signal WRD and read control signal RDD, respectively.

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(54) **MEMORY CIRCUIT AND METHOD FOR READING OUT DATA**

(76) Inventor: **Peter Beer**, Tutzing (DE)

Correspondence Address:
LERNER AND GREENBERG, P.A.
POST OFFICE BOX 2480
HOLLYWOOD, FL 33022-2480 (US)

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(57) **ABSTRACT**

It is possible to read out data in accordance with a read-out address from memory cells via bit lines and primary sense amplifiers. Each secondary sense amplifier is assigned a group of primary sense amplifiers. It is possible for the primary sense amplifiers of a group to be connected to one of the secondary sense amplifiers in each case via switching devices in order to apply the datum from one of the primary sense amplifiers to the assigned secondary sense amplifier via the switching device selected by the read-out address. For reading out data, a test control unit is provided to connect some of the switching devices in parallel depending on a test mode signal and depending on a read-out address, so that in each case one of the group of primary sense amplifiers is connected to the assigned secondary sense amplifiers.